https://dx.doi.org/10.22161/ijaers.4.3.7 *ISSN: 2349-6495(P) | 2456-1908(O)*

Efficient Design of Error Recovery and Improve the Performance Using Mesh of Ring Topology Based NoC

A.Kalimuthu[1], Dr.M.Karthikeyan[2]

[1]Department of ECE, JCT College of Engineering and Technology, Coimbatore, India
[2]Principal, Tamilnadu College of Engineering, Coimbatore, India

Abstract**—** *generally, the System-on-chips (SoCs) is usually an Integrated Circuit in which integrates new elements in a single chip. Because of rise in number of transistors on a single chip gives complex system. To reduce the system complexity integrated SoC within a system, it forms a Network on Chip (NoC). Designed for NoC architectures, high performance efficient router design having minimal power consumption are necessary for real-time applications. NoCs having mesh and Ring structured interconnection topologies now are popular for their simple structures. In this paper, we designed the energy-efficient however high performance approach to conventional Hybrid mesh based-Ring using deflection on-chip networks. Most of us try to achieve the scalability associated with meshes by the router simplicity as well as effectiveness of rings. Our design can be a hierarchical ring interconnect that will keep all the simplicity of conventional ring patterns while reaching high scalability as more complex buffered hierarchical ring designs. We propose a router design and also show these types of routers will be significantly simpler, additional area and power efficient compared mesh based routers. In this work, we all establish the conventional error rates of the on-chip and also designed suitable Error Correction Code (ECC) mechanisms to improve their reliability. We show that using the planned specific ECC method it is easy to achieve significantly reduced power dissipation and high performance in the NoC.*

Keywords— NoC, mesh of ring topology, error correction code (ECC)

I. INTRODUCTION

Although, network-on-chip is really important allow for scalable multi-core processors. A NoC is necessary in selecting over-all process performance because it affects latency moreover bandwidth with overall cost, including power and area. While devices reduce in size towards the nanometer scale, on-chip interconnects have been an important bottleneck in achieving performance and power consumption needs in the chip design. Industry and academia recognize the interconnect difficulties due to the fact involving an important design constrains, as a result, mesh-based Network on Chips (NoCs) are proposed to handle challenges with rising interconnect complexity [5-14]. The Hierarchical Rings structured network-on-chip, consists important features that will allow us to mostly maintain the simplicity of conventional simple ring topologies while supplying larger power effectiveness and also scalability [1-4]. In this paper, we deal with reliability problems inside of a hybrid mesh of ring topology in NoC [4] through proposing a specific Error Correction Code (ECC) structure with various schemes for interconnect links. In the hybrid NoC experience larger error rates compared to regular wires thereby more robust ECC technique need to restore the reliability on this kind of links. During this perform many of us determine the conventional error rates from the on-chip interconnect links and propose appropriate ECC methods to improve their reliability. We show that using the proposed specific ECC scheme it is possible to attain significantly low power dissipation and high performance in a NoC.

II. RELATED WORK

Hierarchical ring based interconnect has been developed in an earlier types of work [14, 15]. We now have by now as compared to previous hierarchical ring scheme performance. The important huge difference between our proposal and this earlier work is we propose deflection-based routers with minimal buffering and also node routers with no buffering; alternatively, most of these previous performs implement routers with in-ring buffering, along with apply wormhole switching and flow control. This really is comparable the difference between buffered mesh routers [16] and bufferless deflection mesh routers [17].

Bufferless Mesh-based Interconnects, while we focus on ring based interconnects to achieve simpler router design and less significant power, further more perform for modifies traditional buffered mesh routers by reducing

https://dx.doi.org/10.22161/ijaers.4.3.7 *ISSN: 2349-6495(P) | 2456-1908(O)*

the buffers and also applying deflection [17]. Even as we present within evaluations, although such types effectively minimize power and area, they support the essential complexity of mesh based routers, and hierarchical ring designs really are a improved overall performance and power.

Other Ring based Topologies, Spidergon [18] proposes a bidirectional ring improved with links in which directly connect nodes opposite one another on the ring. These types of extra links minimize the typical hop range for traffic. But, the cross-ring links develop into extended while the ring develops, avoiding scaling previous particular point, while our design doesn't have such scaling bottleneck. Octagon [21] types a network through combination Spidergon models of 8 nodes each. Designs are joined by dealing with a connection node in common. This kind of design scales linearly. But, it is utilize hierarchy, while our design employs global rings to join local rings. Other Minimal Cost Router Designs, Finally, Kim [20] proposes a low-cost router design that's superficially related to the proposed node router design routers present traffic along rows and columns in a mesh without using crossbars, only pipeline registers and multiplexer. After traffic enters a row or column, it |remain till it reaches their location, as in a ring. Traffic also moves from a row to a column analogously to a ring |move within our design, employing a turn buffer. But, since a turn is possible at any node in a mesh, every router needs this kind of buffer on the other hand, we involve these move buffers just at bridge routers, and their cost is amortized |overall nodes. Mullinset al. [19] proposes a buffered mesh router with single cycle arbitration. We reveal the target of developing a simpler, faster.

1 Evaluation to four standard models

1.1 Buffered mesh,
1.2 Bufferless mesh,
1.3 Single ring,
1.4 Buffered hierarchical ring.
1.5 Mesh of Rings Topology

1.1 Buffered Mesh

A mesh interconnects routes obviously to a 2-D tiled CMP design. Meshes are therefore a typical selection for multi-core CMPs. A mesh topology has excellent performance scalability relative to ring-based types, since their bisection bandwidth develops obviously with the network. On the other hand, single- and hierarchical-ring topologies should expand a ring to maintain sufficient bisection bandwidth. But, a mesh topology allows cross-chip traffic to go to every node along a path. In comparison, a hierarchical topology such as for instance hierarchical ring with deflection (HiRD) enables traffic to corner the chip with fewer hops by utilizing the global ring. A buffered mesh router includes a large complexity and cost compared to the node router at each cache node in the HiRD NoC.In a buffered mesh, each router includes buffers at every router input, and must add a crossbar to move flits from any input to any output. In HiRD, a node router just connects to the ring nodes on each side of the present node, and doesn't have any in-ring buffers. Bridge routers have buffering, but the necessary buffer space is significantly less than in a buffered mesh, and there are fewer bridge routers than nodes in total.

1.2 Bufferless Mesh

Bufferless mesh networks get rid of the buffers from traditional mesh routers, and provide significant energy performance improvements at low-to-medium load. The exact same topology tradeoffs must like the buffered mesh also apply in this case; the improvements produced by a bufferless mesh NoC apply only to the router design itself. A bufferless mesh router is conceptually much like a bridge router in HiRD for the reasons that equally use deflection, since neither router can use backpressure and booth traffic on a router input. In case of HiRD, rings don't have any in-ring buffers, and therefore traffic on rings remains to flow. In case of a bufferless mesh with deflection routing, no router includes in-network buffers, therefore all traffic moves continuously. On the other hand to a bufferless mesh router, a HiRD bridge router includes buffers for traffic that moves between rings. Equally routers include a crossbar. The routing logic in a bufferless mesh router is more complex, as it should consider flit priorities and two dimensional mesh routing. However, despite these tradeoffs, a HiRD system includes fewer bridge routers than nodes, although a bufferless mesh includes this type of router at every node.

1.3 Single Ring

A single ring network has an easier topology when compared to a hierarchical ring. At reduced load, and in small networks, a single ring performs well since each hop includes a reduced latency. But, even as we also show, a ring scales defectively relative to different topologies as load raises or as network size increases. At large load, the lower bandwidth of a ring develops into the main bottleneck, and ring usage rises rapidly. While the network scales up, bisection bandwidth continues to a bottleneck, but the typical number of hops also develops faster than in different topologies: traffic that crosses single-ring network visits half of the nodes throughout their journey, and this will cause high latencies and high power. Developing a network with hierarchy allows show transportation on a global ring, and retains decrease ring use by segmenting the network into multiple local rings.

1.4 Buffered Hierarchical Rings

A buffered hierarchical ring network area local buffering at each node router in a ring. In-ring buffers let the usage

https://dx.doi.org/10.22161/ijaers.4.3.7 *ISSN: 2349-6495(P) | 2456-1908(O)*

of flow control, and bridge routers utilize this flow control to booth inward traffic on a ring whenever move buffer becomes full. On the other hand, HiRD doesn't have flow control in any ring, and must utilize deflections whenever a move buffer fills. Putting buffers in the ring prevents deflections but provides significant buffer area and power to every node router, and also involves flow-control logic at every router in the ring.

1.5 Mesh of Rings Topology

Another method to develop ring topology scalable is always to position local rings in a mesh design as shown in Figure-1.this kind of topology provides the same scalability for a mesh topology, each having complexity proportional to the total number of nodes in the network. The mesh of rings topology also offers the main benefit of easy router design because the essential block node router and bridge router have the same design as these in a hierarchical ring network. As the deadlock and livelock avoidance in mesh of rings topology and we evaluate the performance and power consumption of mesh of rings [4].

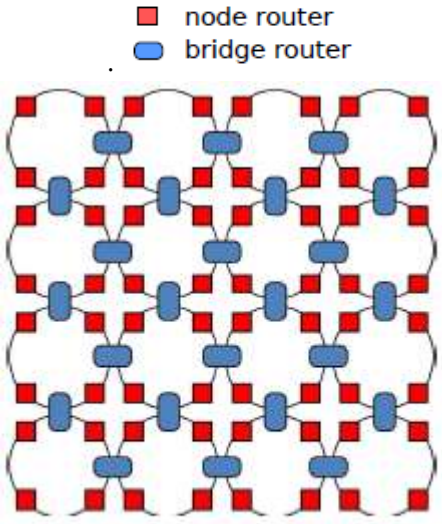

Figure-1Mesh of Rings Topology

III. ROUTER DESIGN

We propose hierarchical mesh of ring Network on chip design based on very simple router architectures to obtain single cycle latencies. Using this method, HiRD, places a typical ring router at most network node, connects local rings with global rings implementing bridge routers, which may have minimal buffering and use deflection instead of flow control for inter ring transfers. We developed with added for Error Correction code (ECC) of traffic ensuring that inter ring moves do not cause livelock or deadlock, even yet in the worst case.

1. Node Router Operation

At each node on a local ring, we position an individual node router, shown in Figure 2. A node router is simple: it moves through circulating traffic, enables new traffic to enter the ring through a multiplexer (MUX), and allows traffic to go the ring when it occurs at their destination. Each one router includes one pipeline register for the router point, and one pipeline register for link traversal, therefore the router latency is exactly one cycle and the per-hop latency is two cycles[1].

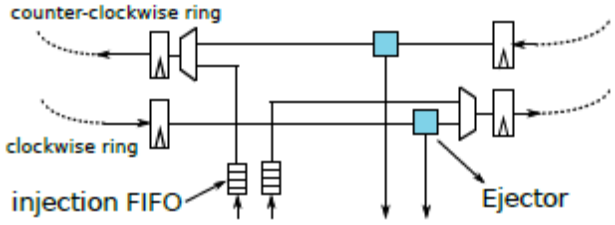

Figure 2: Node router.

2. Bridge Router Operation

The bridge routers link a local ring and a global ring. The high-level block diagram of a bridge router is shown in Figure 3. A bridge router appears like two node routers, one for every one of two rings, linked through FIFO-buffers both in directions. Every time a flit comes on one ring which will requires a move for the ring, it can retain their present ring and also wait in a FIFO provided that there is space available. These types of move FIFOs appear, therefore the moving flit's arrival do not need be completely arranged with a free position on the destination ring. But, this transfer FIFO will often fill. because, if any flit occurs that will requires a move, the bridge router only does not eliminate the flit from their current ring; the flit can continue to travel across the ring, and will ultimately come back to the bridge router, at which stage there may be an open slot available in the transfer FIFO.

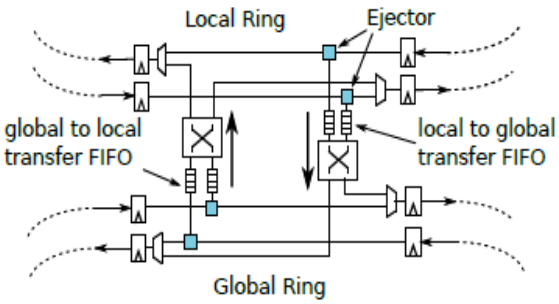

Figure 3: Bridge router.

3. Error detection and correction

The register includes position, data and parity registers needed by router. All the registers in this module are latched on increasing edge of the clock. Data registers latches the data from data input predicated on state and position control signals, and this latched data is delivered to the FIFO for storage. Besides it, data can be latched into the parity registers for parity computation and it is contrast to the parity byte of the packet. Errors indicate is produced if packet parity is not equal to the determined parity. Inner parity register stores the parity determined

https://dx.doi.org/10.22161/ijaers.4.3.7 *ISSN: 2349-6495(P) | 2456-1908(O)*

for packet data, when packet is sent completely, the internal calculated parity is compared with parity byte of the packet.

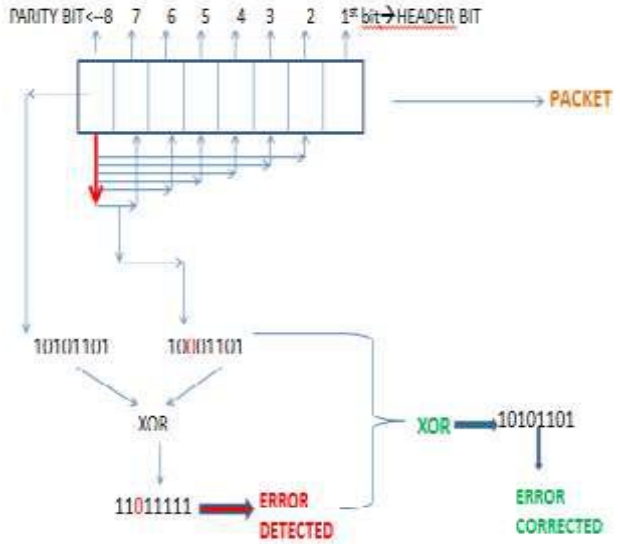

Fig.4: error detection and correction method

IV. RESULT

The NoC router architecture is simulated. In that mesh of ring based NoC the concepts requires a change path to achieve the location even though there is errors in the propagating route. So the message achieves the location even though the router in the transmitting route is faulty. The data sent is free of error as a result of effective exploitation of with error correction code (ECC), by simulation of the ECC module output.

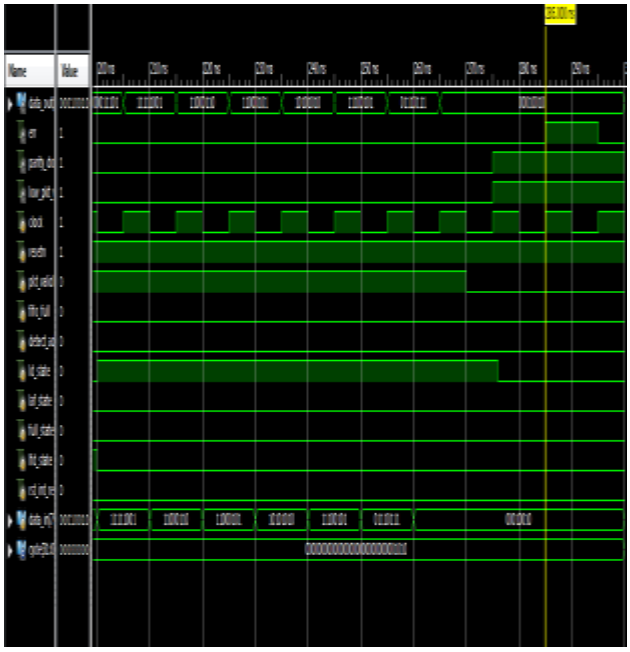

Fig.4: Error detected in the register block of transmitted data.

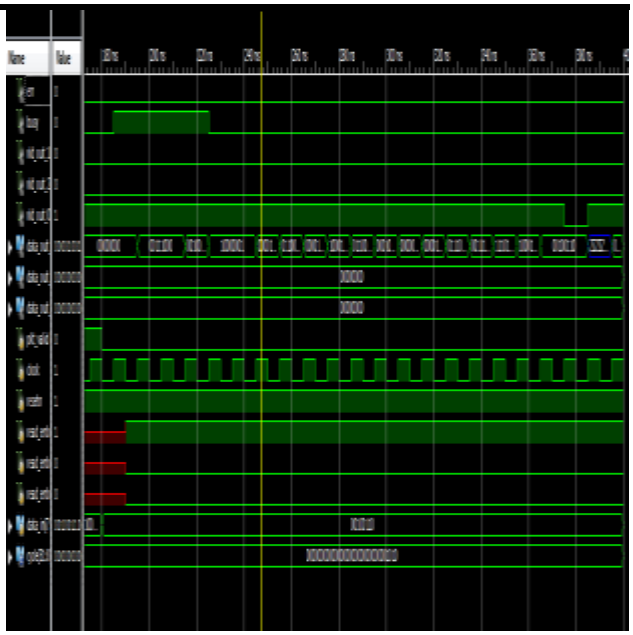

Fig.5: Error corrected in the register block of Received data.

V. CONCLUSION

Our design is a hierarchical ring interconnect that will keep all the simplicity of conventional ring patterns while reaching high scalability as more complex buffered hierarchical ring designs. We propose, a router architectures and show that these routers are significantly simpler, more area and power effective than mesh based routers. In this work we establish the conventional error rates of the on-chip and propose appropriate Error Correction Code (ECC) mechanisms to improve their reliability.

REFERENCES

[1] R. Ausavarungnirun et al. Achieving both High Energy Efficiency and High Performance in On-Chip Communication using Hierarchical Rings with Deflection Routing. In SBAC-PAD, 2016.

[2] C. Fallin, C. Craik, and O. Mutlu. CHIPPER: A low-complexity bufferless deflection router.HPCA-17, 2011

[3] R. Ausavarungnirun et al. Staged Memory Scheduling: Achieving High Performance and Scalability in Heterogeneous Systems. In ISCA, 2012.

[4] Chris Fallin, Xiangyao Yu, Gregory Nazario, Onur Mutlu A High-Performance Hierarchical Ring On-Chip Interconnect with Low-Cost Routers,SAFARI Technical Report No. 2011-007 (September 6, 2011)

[5] D. Bertozzi, L. Benini, G. De Micheli, "Error control schemes for on-chip communication links: the energy- reliability tradeoff," Computer-Aided

https://dx.doi.org/10.22161/ijaers.4.3.7 *ISSN: 2349-6495(P) | 2456-1908(O)*

Design of Integrated Circuits and Systems, IEEE Transactions on , vol.24, no.6, pp.818,831, June 2005

[6] Ganguly, A; Pande, P.P.; Belzer, B., "Crosstalk-Aware Channel Coding Schemes for Energy Efficient and Reliable NOC Interconnects," Very Large Scale Integration (VLSI) Systems, IEEE Transactions on, vol.17, no.11, pp.1626,1639, Nov. 2009.

[7] Cédric Killian, Camel Tanougast, Fabrice Monteiro, and Abbas Dandache, "Smart Reliable Network-on-Chip", IEEE Transactions on Very Large Scale Integration (VLSI) Systems, Vol. 22, No. 2, February 2014

[8] S. Jovanovic, C. Tanougast, S. Weber, and C. Bobda, "A new deadlock-free fault-tolerant routing algorithm for NoC interconnections," in Proc. Int. Conf. Field Program. Logic Appl., Aug.–Sep. 2009, pp. 326–331.

[9] M. Valadbeigi and F. Safaei, "PDR: A Protocol for Dynamic Network Reconfiguration Based on Deadlock Recovery Scheme," in Elsevier Journal of Simulation Modeling Practice and Theory, vol. 24, no.1, 59-70, 2012

[10] D. Park, et al, "Exploring Fault-Tolerant Network-on-Chip Architectures", In Proc. of International Conference on Dependable Systems and Networks, June 2006.

[11] M. Majer, C. Bobda, A. Ahmadinia, and J. Teich, "Packet routing in dynamically changing networks on chip," in Proc. 19th IEEE Int. Parallel Distrib. Process. Symp., Apr. 2005, p. 154b.

[12] Y. Kang, T. Kwon, J. Draper, "Fault-Tolerant Flow Control in On-Chip Networks," in Proc. NoCs, pp.79-86, 2010.

[13] Q. Yu and P. Ampadu, Transient and Permanent Error Control for Networks-on-Chip. Springer, 2012.

[14] X. Zhang and Y. Yan. Comparative modeling and evaluation of CC-NUMA and COMA on hierarchical ring architectures. Parallel and Distributed Systems, IEEE Transactions on, 6(12):1316 –1331, Dec 1995.

[15] V. C. Harmacher and H. Jiang. Hierarchical ring network configuration and performance modeling. IEEE Transaction on Computers, 50(1):1–12, 2001.

[16] W. Dally and B. Towles. Principles and Practices of Interconnection Networks. Morgan Kaufmann, 2004.

[17] T. Moscibroda and O. Mutlu. A case for bufferless routing in on-chip networks. ISCA-36, 2009.

[18] M. Coppola et al. Spidergon: a novel on-chip communication network. Proc. Int'l Symposium on System on Chip, Nov 2004.

[19] R. Mullins et al. Low-latency virtual-channel routers for on-chip networks. ISCA-31, 2004.

[20] J. Kim. Low-cost router microarchitecture for on-chip networks. MICRO-42, 2009

[21] F. Karim et al. On-chip communication architecture for oc-768 network processors. DAC-38, 2001.