

DESIGN AND PERFORMANCE ANALYSIS OF NINE STAGES CMOS BASED RING OSCILLATOR

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ABSTRACT

This paper deals with the design and performance analysis of a ring oscillator using CMOS 45nm technology process in Cadence virtuoso environment. The design of optimal Analog and Mixed Signal (AMS) very large scale integrated circuits (VLSI) is a challenging task for the integrated circuit(IC) designer. A Ring Oscillator is an active device which is made up of odd number of NOT gates and whose output oscillates between two voltage levels representing high and low. There are a number of challenges ahead while designing the CMOS Ring Oscillator which are delay, noise and glitches. CMOS is the technology of choice for many applications, CMOS oscillators with low power, phase noise and timing jitter are highly desired. In this paper, we have designed a CMOS ring oscillator with nine stages. Previously, the researchers were unable to reduce the phase noise in ring oscillators substantially with nine stages. We have successfully reduced the phase noise to -6.4kdBc/Hz at 2GHz center frequency of oscillation.

KEYWORDS

Analog and mixed signal (AMS), VLSI circuit, CMOS Ring oscillator (RO), integrated circuit (IC), phase noise, center frequency of oscillation

1. INTRODUCTION

The ring oscillator is the most widely manufactured integrated circuit of all. Ring oscillators are being used by semiconductor foundries on every semiconductor wafer to monitor the power dissipation, delay, jitter of fabricated CMOS inverters. A particular measurements pattern of oscillation frequency determines which wafers are to be accepted and which are to be rejected. The ring oscillator is basically a closed loop comprised of an odd number of identical inverters, which form an unstable negative feedback circuit. The period of oscillation of ring oscillator is the twice the sum of the gate delays in the ring comprises of inverters. A voltage controlled ring CMOS inverter based oscillator is first used for clock recovery in an Ethernet controller [1]. Since then, the ring oscillator has become a widely used component in the communication. Now a days, almost all ring oscillators use differential delay stages [2], because of their greater immunity to supply disturbances. Thus, the ring oscillator is comparatively very compact as compared to LC resonator based oscillator. A significantly large number of ring oscillators take up the very small

chip area. It can also oscillate at very high frequencies i.e.; at very short periods limited only by the sum of a few gate delays. The maximum oscillation frequency of ring oscillator is always higher than the relaxation oscillator. There has been a stream of publications since the early 80s on analytical estimation of delay in chains of CMOS inverters, and since the mid 90s on estimation of jitter in ring oscillators. However, the analysis for gate delay becomes increasingly non intuitive as it gets more accurate, and the latest editions of textbooks on VLSI designs [3],[4]

hold that is better to use the simplest possible analysis for a first order estimate of gate delay and then refine it with simulation. VCO is the most important part of the PLL. It generates the required frequency. The VCO used in the PLL is a ring oscillator having nine differential buffer stages.

1.2. CMOS DELAY

Propagation delay (t_d) is defined as the time between when the input crosses the switching threshold [3] or toggle point (V_M) of the inverter to when its output crosses the toggle point of next inverter in a chain. The first publications on the subject estimated delay by the time for the output voltage of an NMOS and CMOS inverter driving the capacitance of the next stage to cross the trip point in response to an input step [Fig. 3(a)]. However, the input waveforms in a practical logic chain are not ideal steps but have a finite slope, which in the case of a chain of identical stages is the same at the input and output of each inverter with opposite sign. This has led to a refined calculation based on step response delay which takes into account of the finite slope of the input ramp [6][fig. 3(b)]. Generally, for large fanouts, a longer propagation delay than an input step is calculated.

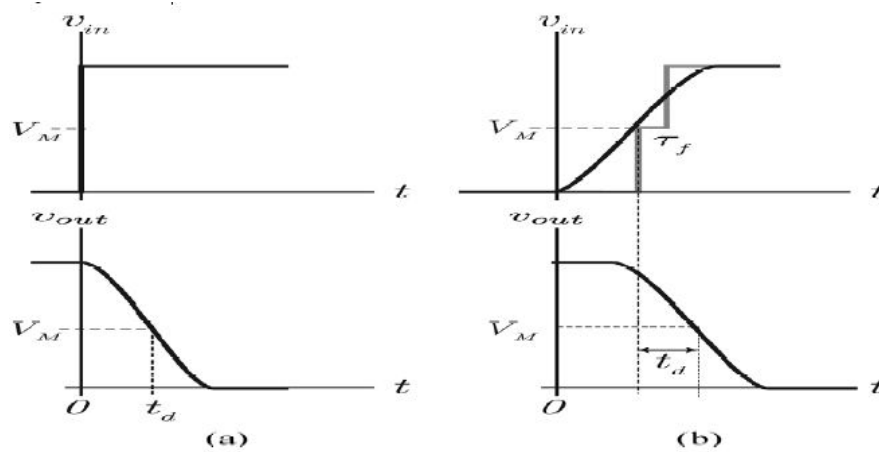


Figure 3. (a) Propagation delay defined in response to a step voltage input.
(b) Realistic ramp input, which can be approximated by a two-step input for any fanout [17].

Yet better estimates of propagation delay continue to be published; for example, [7] gives a surprisingly complicated but complete analytical expression for delay, given that the circuit in question contains only an NFET, a PFET, and a capacitor. The complexity of these analyses forces designers to continue to use imple estimates based on RC delay for hand calculation, which are refined on timing simulations[3],[4]. When the fanout is one as in a ring oscillator simple but reasonably accurate models of dynamics can suffice. In [8] it is shown that delay can be estimated within 10% by approximating a ramp with a delayed two level step input. The delay in the first step is the time it takes the ramp to reach the inverter toggle point, and the delay in the second step depends on the load capacitance and the ramp rate at the input.

1.3 RING OSCILLATOR JITTER

The first paper estimates jitter caused by FET noise in CMOS differential ring oscillators [9] cast the problem correctly in the time domain, by finding fluctuations in the instants when the output

ramp in a delay element crosses the toggle point. This is similar to the analysis used to find jitter and phase noise depends on the voltage gain of the delay circuit. Experience tells us that voltage gain of the delay element should not matter as long as it is large; indeed, it can be infinite because delay and therefore jitter depend mainly on charge and discharge current and capacitance. It also gave the correct expression that links period jitter which we will define below with phase noise; subsequent analyses, including our own, show that this relationship holds for white noise sources. The paper does not address flicker noise. The second paper analyses the jitter focused on ring oscillator using ECL like BJT delay stages [11]. The analysis as well as the results were in the time domain, again defining jitter by fluctuations in instants of threshold crossings at each delay stage in a closed chain. There was no attempt to link jitter to phase noise. Both the papers take into account the time varying nature of the circuit by first analyzing the steady state RMS noise at equilibrium, with the load RC setting the noise bandwidth; and modeling exponential decay or builds up with this time constant to capture the time varying aspect of the large signal switching. The next paper [12] applies the concept of the impulse sensitivity function to the waveforms of a ring oscillator and from relation between the impulse sensitivity function and phase noise, deduces an approximate expression for phase noise. The latest analysis of the ring oscillator phase noise [13] explores details of the noise processes at the toggle point of the delay element but at the end offers no analytical expressions, simple or otherwise, for the phase noise or jitter. With this as background, this paper presents a comprehensive analysis of jitter and phase noise in both CMOS inverter based and differential ring oscillators, pinpointing the most important mechanisms whereby white and flicker noise manifest themselves. The physically based approach and simple resulting expressions should make it easy to design ring oscillators for a given jitter [14].

$$f_{osc} = 1 - \frac{1}{\eta \cdot N \cdot (t_r + t_f)} = \frac{I_D}{\eta \cdot N \cdot C_{total} \cdot V_{DD}} \quad 1$$

$$C_{total} = \frac{5}{2} C_{ox} (L_p W_p) + (L_n W_n) \quad 2$$

2. SYSTEM DESIGN

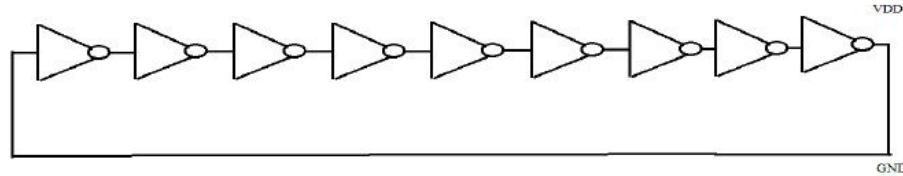


Figure 1. Proposed Block Diagram of 9 stages CMOS Ring Oscillator

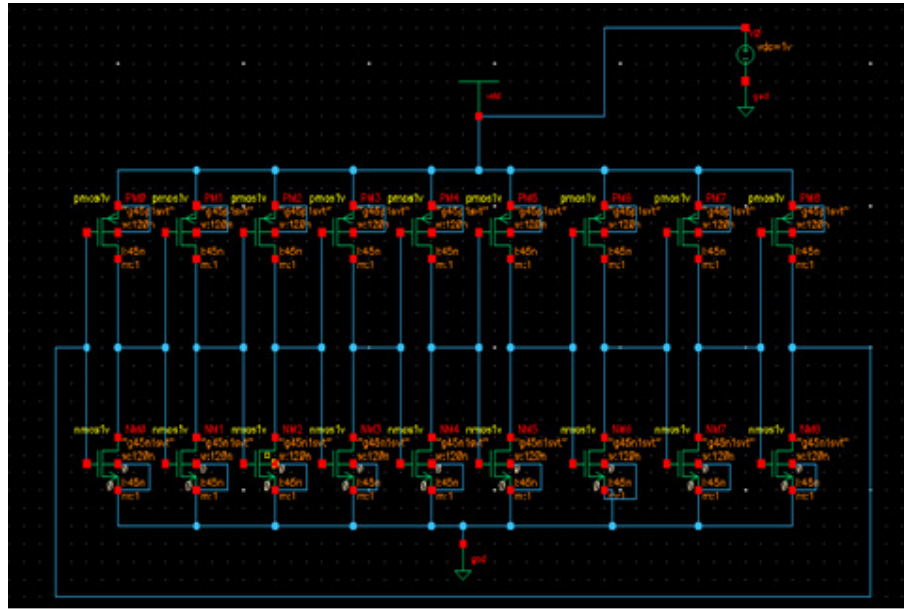


Figure 2. Schematic diagram of 9 stages CMOS Ring Oscillator



Figure 3. One of the stages of 9 stages CMOS Ring Oscillator

The design entry of the circuits is carried out in the schematic editor of Cadence Virtuoso Analog Design Environment using gpd45 library. For performance analysis these circuits are simulated in Spectre simulator of Cadence tool. The transistor sizes obtained as above for a set of specifications are used to design the required ring oscillator circuit. The first ring oscillator is designed for nine stages of CMOS inverters and the W/L ratio which is 45nm CMOS Technology.

Table 1. Design Parameters of 9 stages Ring Oscillator

W_p (nm)	120
W_n (nm)	120
L (nm)	45

Even numbered circular inverter chain cannot be used as a ring oscillator because the eventual or ultimate output is same as input in this case. Although, this sort of inverter configuration can be used as a data storage element between input and output. A ring oscillator can comprise of a mixture of inverting and non - inverting stages of nand gate but the number of stages should be odd like; 9, 11 etc. The oscillation period of ring oscillator is equal to the twice the sum of each and every individual stage delays. The ring oscillator must have the gain of greater than 1 at the intended frequency of oscillation. Even a small noise can cause the ring oscillator output to rise slightly. After having passed through the element of time delay, this small output voltage change will be clearly visible to the ring oscillator input. The negative gain of more than 1 for ring oscillator means that the output will change in the direction opposite to this input voltage. A change will be observed by an amount larger than the input value for a ring oscillator gain of greater than 1. A real ring oscillator only requires only power to operate; above a certain threshold voltage oscillations begin spontaneously. The increase in the number of stages of inverters in ring oscillator increases the total delay and thus decreases the frequency of oscillation. Also, higher supply voltage decreases the delay and increases the frequency of oscillation.

3. RESULTS AND ANALYSIS

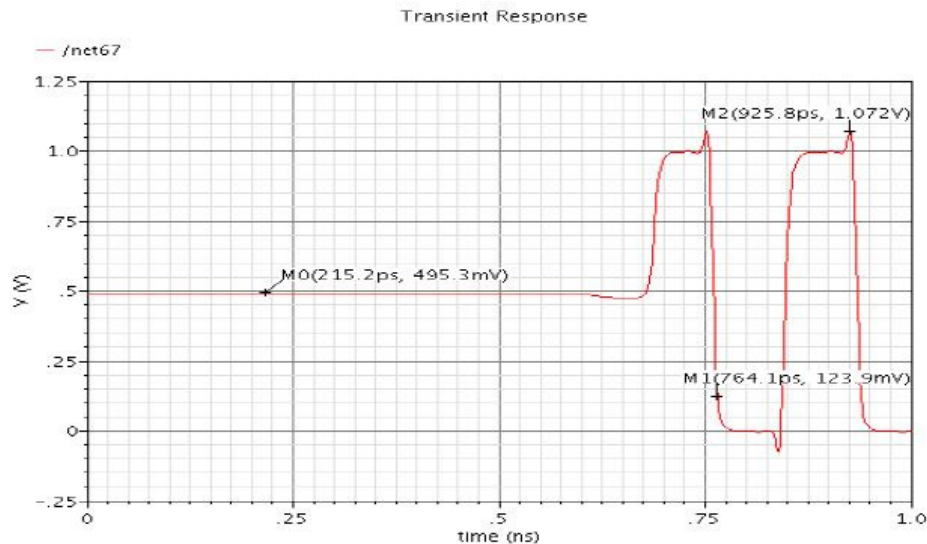


Figure 4. Waveform for Transient Analysis of 9 stages CMOS Ring Oscillator

In figure 4, a transient analysis was performed to illustrate the effects of the parasitic parameters over the oscillation frequency and to observe the behavior of the waveform with respect to time e.g; for point M1, 123.9 mV supply voltage is used at 764.1 ps by the 9 stages Ring Oscillator.

This kind of result is due to glitches in the waveform.

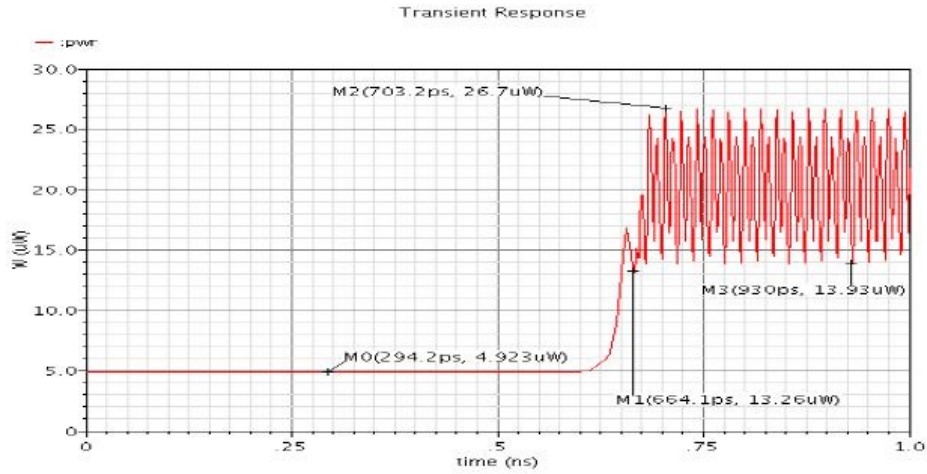


Figure 5. Waveform for Power consumption of 9 stages CMOS Ring Oscillator

The above figure is for the power for 9 stage Ring Oscillator and for point M2, 26.7 uW power dissipated at 703.2 ps and average power dissipated is 10.15×10^{-6} W. Till this point, the curve of power consumed is linear because the CMOS transistor takes time to stabilize itself and after this point, a typical waveform for power consumed by Ring Oscillator is obtained which is drastically changing even a small change in time due to parasitic of the CMOS transistor.

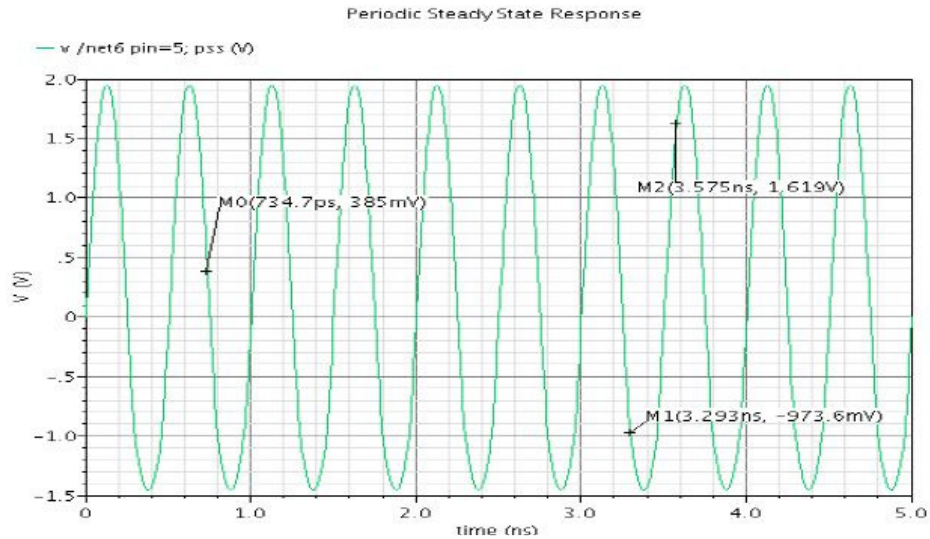


Figure 6. Waveform for Voltage of 9 stages CMOS Ring Oscillator

Waveform shown above is of 9 stages Ring Oscillator for the voltage in volts with respect to the PSS response over a period of 5 ns. At point M0 i.e; at 734.7 ps, the voltage is 385 mV which is in agreement to the expected theoretical values because of the sinusoidal nature (chosen as option) of the supply voltage in the given case.

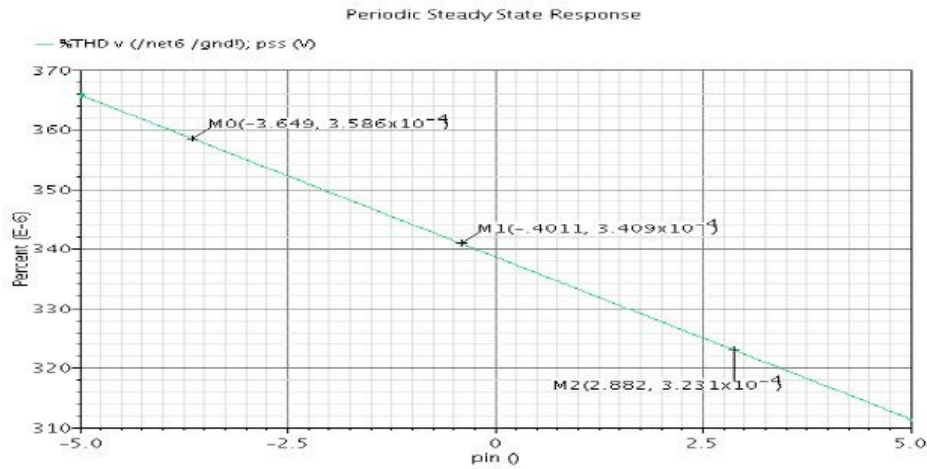


Figure 7. Waveform for THD of 9 stages CMOS Ring Oscillator

It is known from the above figure that the total harmonic distortion (THD) with respect to the PSS response over a range varying from -5 to 5. At point M0 i.e; at -3.649, the total harmonic distortion (THD) is 3.586×10^{-4} and at point M1 i.e; at -.4011, the total harmonic distortion (THD) is 3.409×10^{-4} . THD is the measurement of the distortion created from the RO's current draw. Lesser THD, for example, allows the components in a loudspeaker, amplifier or microphone or other equipment to make a violin sound like a violin when played back. THD is used to characterize the linearity of audio systems and the power quality of electric power systems.

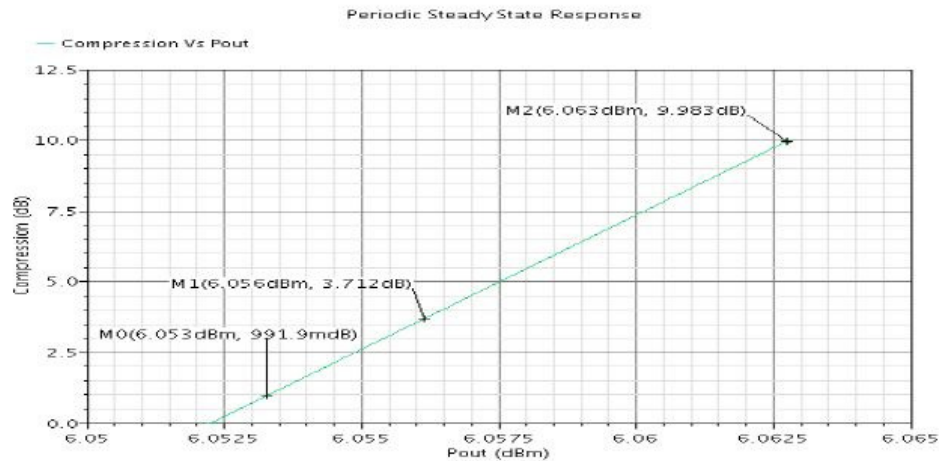


Figure 8. Waveform for Compression Point of 9 stages CMOS Ring Oscillator

The waveform shown above is of 9 stages Ring Oscillator for compression point the with respect to the PSS Response over a range varying from 6.05 to 6.065. At point M2 i.e; at 6.063 dBm, the value of compression point is 9.983 dB. At some power level, the gain response of the device is reduced by a specific amount. This power level is called the compression point.

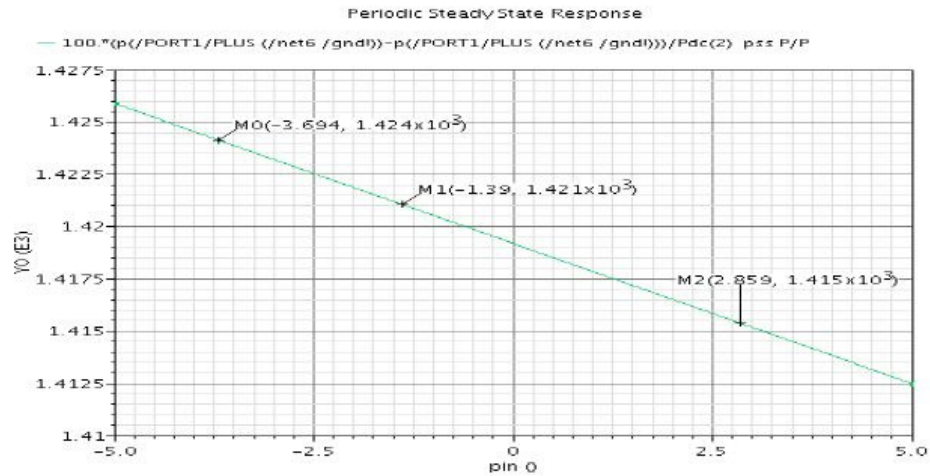


Figure 9. Waveform for Power Added Efficiency of 9 stages CMOS Ring Oscillator

Waveform shown above is of 9 stages Ring Oscillator for the power added efficiency with respect to the PSS Response over a range varying from -5 to 5. At point M0 i.e; at -3.694, the power added efficiency is 1.424x10³ and at point M2 i.e; at 2.859, the power is 1.415 x10³. Power Added Efficiency is basically method to rate the efficiency of power devices like ring oscillator.

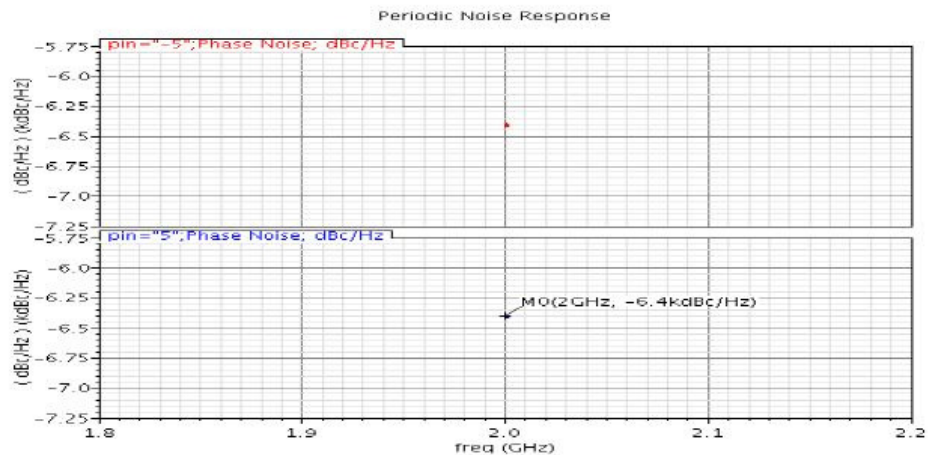


Figure 10. Waveform for Phase Noise of 9 stages CMOS Ring Oscillator

Waveform shown above is of 9 stages Ring Oscillator for the phase noise with respect to the PSS response over a range varying from 1.8 to 2.2. At point M0 i.e; at 2 GHz, the phase noise is -6.4 kdBc/Hz. Phase Noise is the random or sudden fluctuation in the phase of a waveform in frequency domain.

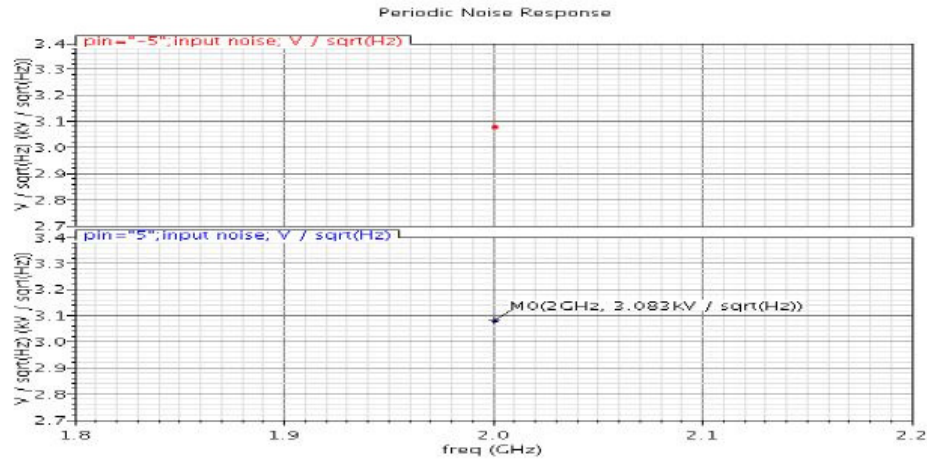


Figure 11. Waveform for Input Noise of 9 stages CMOS Ring Oscillator

The figure shown above is of 9 Stage Ring Oscillator for the input noise with respect to the PSS response over a range varying from 1.8 to 2.2. At point M0 i.e; at 2 GHz, the input noise is 3.083kV/sqrt(Hz). It is actually a measure of how much noise a mic preamp will add to a microphone's signal.

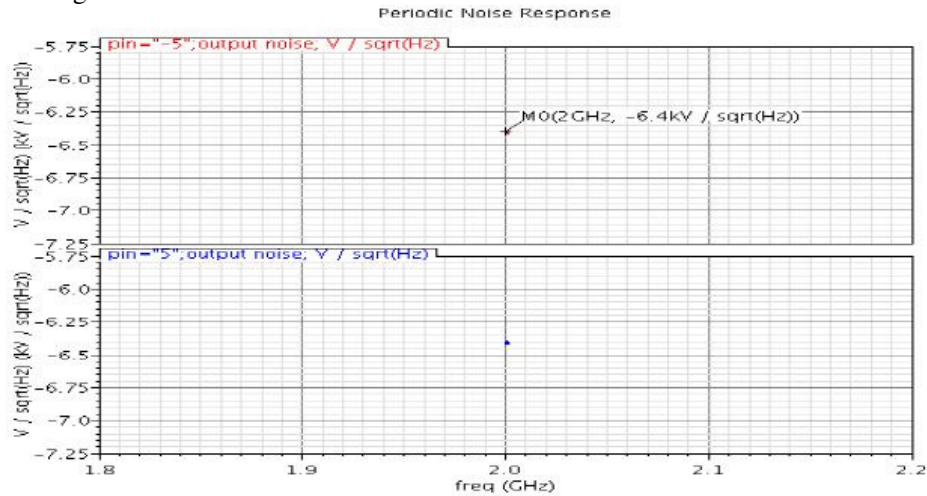


Figure 12. Waveform for Output Noise of 9 stages CMOS Ring Oscillator

Waveform shown above is of 9 stages Ring Oscillator for the output noise with respect to the PSS response over a range varying from 1.8 to 2.2. At point M0 i.e; at 2 GHz, the output noise is - 6.4 kV /sqrt(Hz).

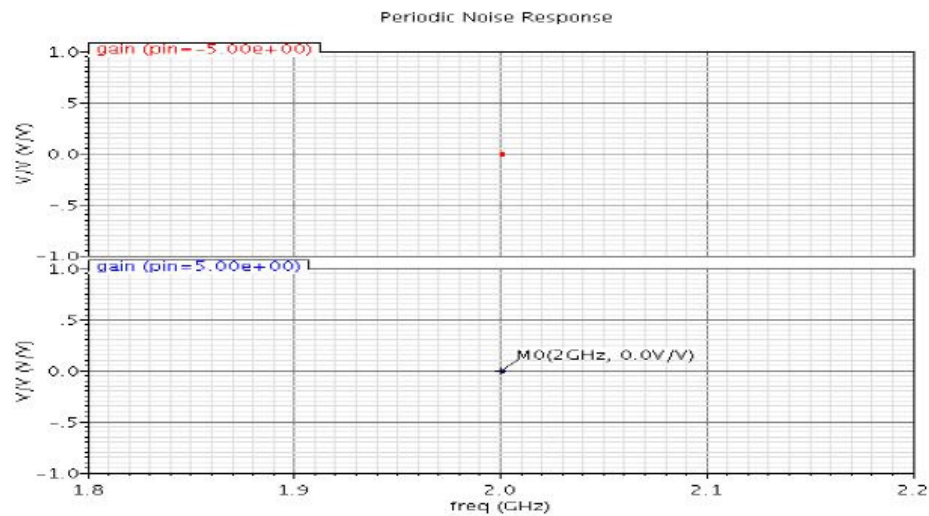


Figure 13. Waveform for Transfer Function of 9 stages CMOS Ring Oscillator

The waveform shown above is of 9 stages Ring Oscillator for the transfer function with respect to the PSS Response over a range varying from 1.8 to 2.2. At point M0 i.e; at 2 GHz, the transfer function is 148.5 nV /V. Transfer functions are commonly used in the analysis of systems such as single input single output filter. The term is often used to refer to Linear Time Invariant Systems (LTI).

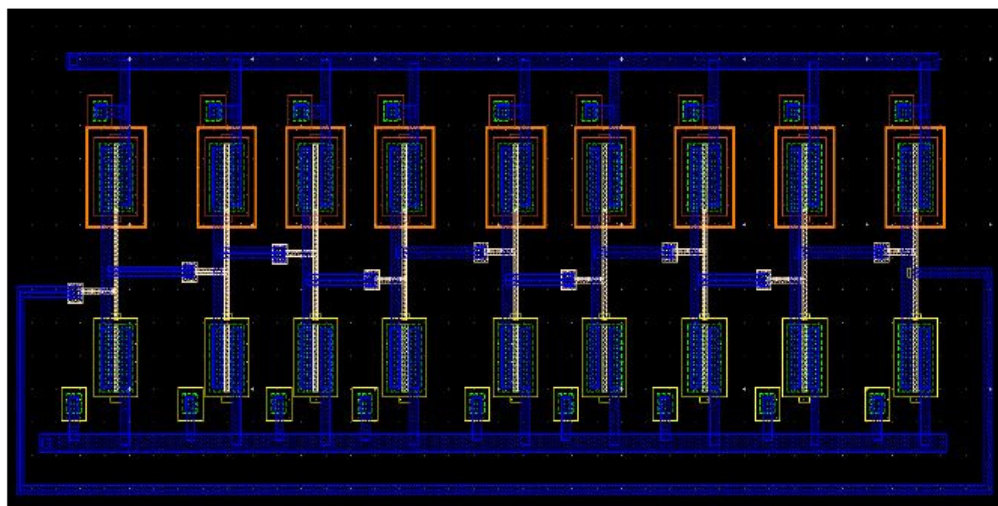


Figure 14. Layout of 9 stages CMOS Ring Oscillator in 45nm CMOS Technology

Table: 2 Performance Parameters of 9 stages Ring Oscillator

Performance Parameters	Ring Oscillator with 9 stages
Average Power	10.15×10^{-6} W
Frequency	5.63 GHz
Phase Margin	180 degree
Bandwidth	684.0×10^{12} b/s
Frequency Jitter	100MHz at 800 ps
Period Jitter	0 s at 933.5 ps
Voltage	3.85 mV at 734.7 ps
Harmonic Frequency	2 GHz
Phase Noise	-6.4 kdBc/Hz
Input Noise	3.083 kV/sqrt(Hz) at 2 GHz
Output Noise	-6.4 kV/sqrt(Hz) at 2 GHz
Total Harmonic Distortion(THD)	3.586×10^{-4} at -3.649
Noise Factor	1 V ² /Hz at 2 GHz
Transfer Function	0.0 V/V at 2 GHz
Power Added Efficiency	91.424×10^{-5} at point - 3.694
Compression Point	3.712 dB at 6.056 dBm
IPN Curves	1 dB/dB at first order

A transient analysis (TA) is performed to illustrate the effects of the parameters over the oscillation frequency and to observe the behavior of the waveform with respect to time. Periodic steady state (PSS) analysis is generally done to determine the oscillation frequency and the influence of the parameters such as power dissipation, noise, supply voltage etc. which have been discussed above. PNOISE analysis normally calculates frequency convention effects and noise folding.

4. CONCLUSION

The nine stages CMOS ring oscillator design has successively been designed and executed using CMOS 45nm technology process in Cadence virtuoso environment. Also, various performance parameters like noise, delay, glitches etc. were analysed and reduced accordingly to optimize the efficiency of the nine stages ring oscillator. We improvised the previous research work by the

author by obtaining the value of period jitter 0 at 933.5 ps, phase noise -6.4 kdBc/Hz, Total Harmonic Distortion (THD) 3.586×10^{-4} at point -3.649 and Power Added Efficiency 91.424 x103 at point -3.694.

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