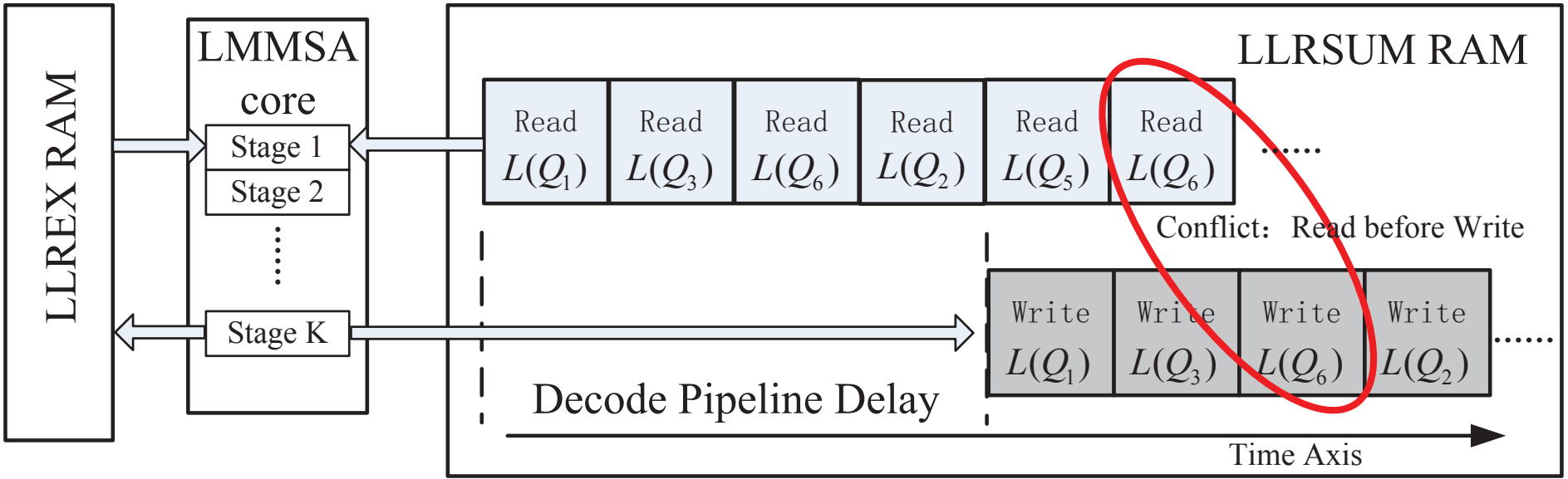
LLREX RAM
LMMSA core
Stage 1
Stage 2
Stage K
LLRSUM RAM
Read $L(Q_1)$
Read $L(Q_3)$
Read $L(Q_6)$
Read $L(Q_2)$
Read $L(Q_5)$
Read $L(Q_6)$
Conflict: Read before Write
Write $L(Q_1)$
Write $L(Q_3)$
Write $L(Q_6)$
Write $L(Q_2)$
Decode Pipeline Delay
Time Axis